17.8 A Miniature V-band 3-Stage Cascode LNA in 0.13μm CMOS

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RF MOSFET technology is maturing, owing to the scaling of MOSFETs, with unity current gain frequencies (f_T) being comparable to those of GaAs-based HEMT technologies. Millimetre-wave (MMW) LNAs are important and widely used in high-frequency front-end circuits. A MMW LNA in 0.13μm CMOS is presented in [1] with a small signal gain of 12dB at 60GHz using devices with f_{max} of 135GHz. Although the lossy substrate in CMOS technology is still a critical design issue, CMOS is still desired for microwave/MMW wireless communication systems due to the capability of integration with IF and baseband circuits. In this paper, a V-band LNA is designed, fabricated and tested using a 0.13μm bulk CMOS process, which provides MIM capacitors, 1P8M with ultra-thick top metal of 3.3μm. The CMOS process features f_{max} and f_T of 108 and 91GHz, respectively. The measurement results of this LNA circuit indicates that standard bulk CMOS technology is suitable for high-gain MMW applications.

In LNA design, the cascode device configuration is utilized to achieve high gain performance. In order to obtain the maximum small signal gain from the cascode structure, the size of the common source (CS) and common gate (CG) NMOS transistors can be crucial for a high gain amplifier design. The maximum stable power gain (MSG) of different combinations of the CS and CG transistor sizes for a cascode NMOS configuration compared with a common source NMOS are shown in Fig. 17.8.1. It is observed that the cascode NMOS pair with 18-finger CS MOS and 36-finger CG MOS (each with 2μm unit finger length) exhibits a higher MSG at 60GHz than the MSGs of other combinations of the cascode NMOS pairs (CS and CG both using 18-finger devices and both using 36-finger devices), and also much higher than that of a single common source device. Although the MSG of the cascode NMOS using a 6-finger CMOS in both CS and CG devices exhibits a slightly higher value than one used in our V-band LNA design (18-finger CS and 36-finger CG), the input impedance of a 6-finger cascode NMOS pair is a little too high to implement the matching circuits. The circuit schematic diagram is shown in Fig. 17.8.2, which consists of three cascode stages. All the input, output and inter-stage matching networks are conjugately matched for maximum small signal gain. Each stage consumes 11mA current at 2.4V bias, with a total dc power consumption of 79mW.

In order to overcome the lossy silicon substrate and the no backside ground issues in the MMW RFIC designs using bulk CMOS processes, the matching networks were usually implemented using thin film microstrip (TFMS) lines [10,11] or co-planar waveguides (CPW) [1,4,6-11]. Although it is still debatable whether the TFMS lines or CPW has lower loss on bulk Si substrate for MMW applications [1,2,11], the TFMS line is advantageous in the circuit layout due to the large ground plane of CPW. On the other hand, because of the thin oxide layer as the substrate, the TFMS lines can be meandered in a very compact manner without suffering the coupling effect. In this circuit, the TFMS lines are adopted to implement the matching networks for a compact layout. Figure 17.8.3 illustrates the chip micrograph of the fabricated V-band LNA. The spaces between lines are more than three times the substrate thickness to avoid coupling effects. The input and output probe pads are designed as small as possible to reduce the parasitic capacitances, so as not to degrade the high frequency performance. Dummy metal layers are kept away from the signal line so as not to disturb the transmission signal field. The chip size is 0.72×0.67mm^2, including all testing pads and dummy metal.

The V-band LNA chip was measured via on-wafer probing. Figure 17.8.4 plots the measured small signal gain and input/output return losses from 40 to 70GHz at 2.4V drain bias with total current of 33mA. The measured gain is higher than 20dB from 51 to 57.5GHz with a peak gain of 24.7dB at 56.1GHz. The input and output return losses are better than 8 and 5dB, respectively. The measured noise figure at the same bias condition is shown in Fig. 17.8.5, and exhibits an average noise figure of 8dB from 50 to 57GHz, with a minimum of 7.1dB at 56.8GHz. The small signal gain performance at different bias conditions are also plotted in Fig. 17.8.6. It achieves a maximum gain of 26.4dB at 2.6V drain bias with a total current of 34mA. Under 2.4V/33mA bias condition, the input 1dB compression point (P_{1dB}) is –22dBm and input IP3 is –12dBm at 56GHz. The saturated output power is 5dBm at 56GHz.

Figure 17.8.7 summarizes the previously reported MMW V-band LNAs compared with this design. It is observed that this LNA achieves a respectable gain performance, even comparable to those of V-band InP-based HEMT LNAs, with a much smaller chip size. It also outperforms all the reported CMOS amplifiers in the V-band, with the highest gain, the lowest noise figure, and smallest chip size, and represents state-of-the-art results among the reported MMW CMOS LNAs.

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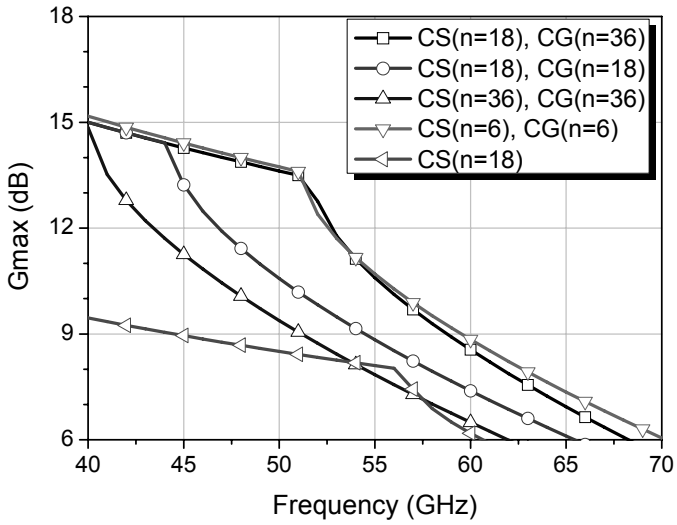

Figure 17.8.1: Comparison of maximum available gain of different cascode and CS transistors (finger width = 2μm, n = finger number).

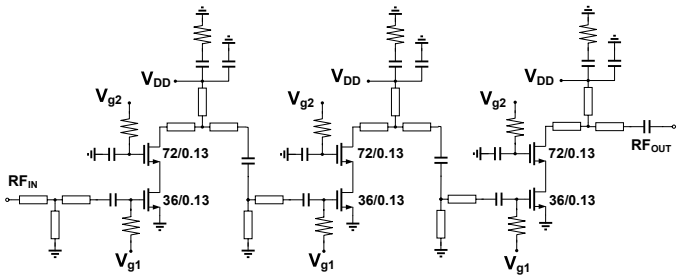

Figure 17.8.2: Circuit schematic of the V-band CMOS LNA.

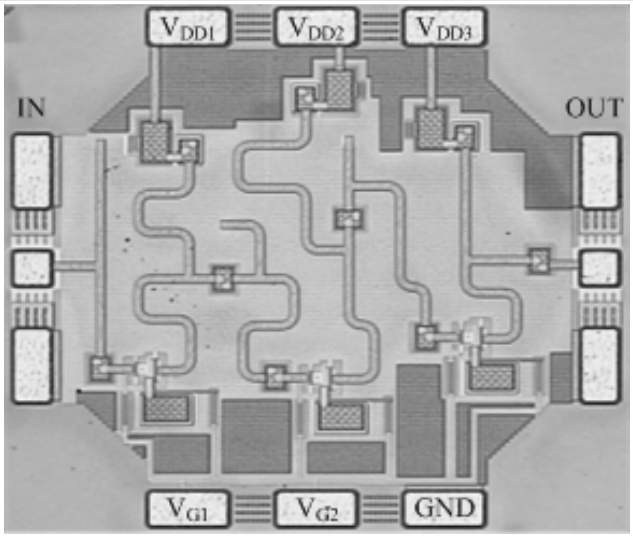

Figure 17.8.3: The chip micrograph of V-band CMOS LNA with die size of 0.72×0.67mm².

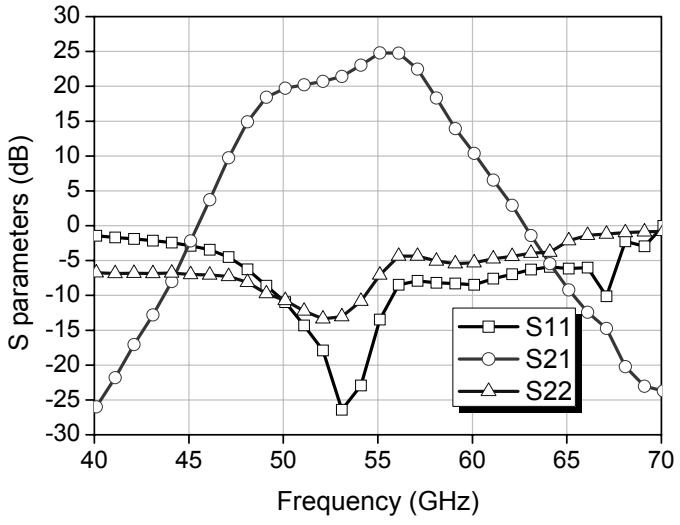

Figure 17.8.4: The measured S parameters (Bias at Vdd=2.4V Id=33mA).

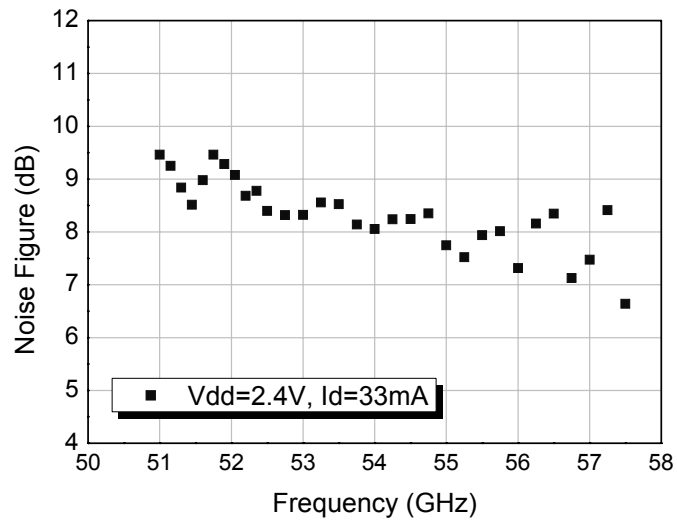

Figure 17.8.5: The measured noise figure (Bias at Vdd=2.4V Id=33mA).

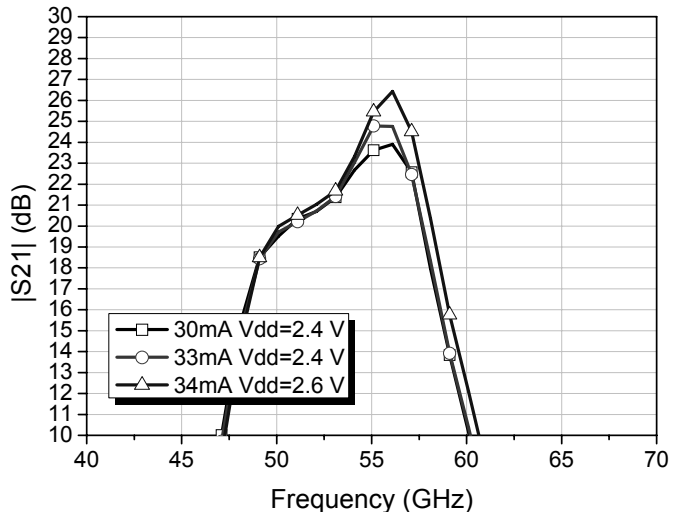

Figure 17.8.6: Measured small signal gain at different bias conditions.

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Techology (Design feature)	Freq. (GHz)	Gain (dB)	NF (dB)	Chip size (mm^2)	Power (mW)	P_{1dBout} (dBm)	Ref. / Year
0.18 µm InP HEMT (3-stage CS)	50-68	15	6	4.2	30	N/A	[2] / 2000
0.1 µm InP HEMT+ (3-stage CS)	56-64	24	3	6.7	20	N/A	[3] / 1993
0.15 µm GaAs pHEMT+ (4-stage CS)	51	42	3	N/A	72	7.7 @51GHz	[8] / 1995
0.15 µm GaAs pHEMT+ (2-stage CS)	49-52	20	2.5	N/A	24	N/A	[8] / 1995
0.15 µm GaAs pHEMT (5-stage CS)	59-62	20	N/A	N/A	100	N/A	[9] / 2003
0.12 µm SiGe HBT (1-stage CG + Cascode)	56-64	15	4.5	0.54	11	-5 @61GHz	[7] / 2005
0.12 µm SOI CMOS (9-stage DA)	0-90	11	4.8-6.2 <18GHz	1.28	210	12 @20GHz	[5] / 2004
0.13 µm CMOS (3-stage Cascode)	51-65	12	8.8	1.3	54	2 @60GHz	[1] / 2005
0.13 µm CMOS (3-stage Cascode)	31-44	19	N/A	1.43	36	-0.9 @38GHz	[1] / 2005
0.09 µm CMOS (2-stage CS)	38-40	6	6	0.7	19	0 @40GHz	[4] / 2004
0.09 µm CMOS (CMSDA)	0-70	7	6-6.9 < 25GHz	0.72	122	10 @30GHz	[6] / 2004
0.13 µm CMOS (3-stage Cascode)	**50-58**	**24.7@ 56GHz >20 (51-57GHz)**	**7.1@56.8GHz ~8 (51-57GHz)**	**0.46**	**72**	**1.8 @56GHz**	**This work**

+ packaged

Figure 17.8.7: Comparison of previously reported V-band LNAs.

